| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 1 | 0 | 10/064869 | USPAT | 2004/04/13 12:12 |
| 2 | 52662 | DRAM and FET and (dual adj gate) and (plate adj electrode) dielectric and capacitor or storage and gate and material and oxide | USPAT | 2004/04/13 12:16 |
| 3 | 43887 | DRAM and FET and (dual adj gate) and (plate adj electrode) dielectric and capacitor or storage and gate and material and oxide and memory and stacked and SOI and buried and plurality and cell and expose | USPAT | 2004/04/13 12:18 |
| 4 | 43867 | DRAM and FET and (dual adj gate) and (plate adj electrode) dielectric and capacitor or storage and gate and material and oxide and memory and stacked and SOI and buried and plurality and cell and expose and pair and trench and doping and dope | USPAT | 2004/04/13 12:23 |
| 5 | 43867 | DRAM and FET and (dual adj gate) and (plate adj electrode) dielectric and capacitor or storage and gate and material and oxide and memory and stacked and SOI and buried and plurality and cell and expose and pair and trench and doping and dope and etch and etching and (enhanced adj soft adj error) | USPAT | 2004/04/13 12:24 |
| 6 | 14 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor or storage and gate and material and oxide and memory and stacked and SOI and buried and plurality and cell and expose and pair and trench and doping and dope and etch and etching and (enhanced adj soft adj error) | USPAT | 2004/04/13 12:26 |
| 7 | 0 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and storage and gate and material and oxide and memory and stacked and SOI and buried and plurality and cell and expose and pair and trench and doping and dope and etch and etching and (enhanced adj soft adj error) | USPAT | 2004/04/13 12:27 |
| 8 | 0 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and storage and gate and material and oxide and memory and stacked and SOI and buried and plurality and cell and expose and pair and trench and doping and dope and etch and etching | USPAT | 2004/04/13 12:27 |
| 9 | 0 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and storage and gate and material and oxide and memory and SOI and buried and plurality and cell and expose and pair and doping and dope and etch and etching | USPAT | 2004/04/13 12:28 |
| 10 | 10 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and doping | USPAT | 2004/04/13 12:31 |
| 11 | 0 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and storage and gate and memory and SOI and plurality and cell and expose and pair and doping and dope and etching | USPAT | 2004/04/13 12:29 |
| 12 | 0 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and storage and gate and memory and SOI and plurality and cell and expose and pair and doping and etching | USPAT | 2004/04/13 12:29 |
| 13 | 0 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and storage and gate and memory and SOI and plurality and cell and expose and doping and etching | USPAT | 2004/04/13 12:29 |
| 14 | 0 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and storage and gate and memory and SOI and plurality and cell and doping and etching | USPAT | 2004/04/13 12:30 |

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| 15 | 0 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and storage and gate and memory and plurality and cell and doping and etching | USPAT | 2004/04/13 12:30 |
| 16 | 0 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacit r and gate and memory and plurality and cell and doping and etching | USPAT | 2004/04/13 12:31 |
| 17 | 0 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacit r and gate and memory and plurality and cell and doping | USPAT | 2004/04/13 12:31 |
| 18 | 10 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and doping and etching | USPAT | 2004/04/13 12:31 |
| 19 | 10 | DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and doping and etching and storage | USPAT | 2004/04/13 12:32 |
| 20 | 10 | (DRAM and FET and (dual adj gate) and (plate adj electrode) and dielectric and capacitor and doping and etching and storage) and (memory or cell or portion or first or second or all or height or 0.15 or microns or plurality or expose or exposed or side or buried or oxide or insulator or capacitor or FET or rails or pair or electorde or gate) | USPAT | 2004/04/13 12:49 |
| 21 | 1 | ("6064588").PN. | USPAT | 2004/04/13 12:49 |
| 22 | 1 | (("6064588").PN.) and (memory or cell or portion or first or second or all or height or 0.15 or microns or plurality or expose or exposed or side or buried or oxide or insulator or capacitor or FET or rails or pair or electorde or gate or DRAM or dual or gate or soft or error or enhanced or dielectric or substrate or plate) | USPAT | 2004/04/13 12:52 |
| 23 | 1 | ("4641165").PN. | USPAT | 2004/04/13 12:52 |
| 24 | 1 | (("4641165").PN.) and (memory or cell or portion or first or second or all or height or 0.15 or microns or plurality or expose or exposed or side or buried or oxide or insulator or capacitor or FET or rails or pair or electorde or gate or DRAM or dual or gate or soft or error or enhanced or dielectric or substrate or plate) | USPAT | 2004/04/13 12:54 |
| 25 | 1 | ("6077745").PN. | USPAT | 2004/04/13 12:53 |
| 26 | 1 | (("6077745").PN.) and (memory or cell or portion or first or second or all or height or 0.15 or microns or plurality or expose or exposed or side or buried or oxide or insulator or capacitor or FET or rails or pair or electorde or gate or DRAM or dual or gate or soft or error or enhanced or dielectric or substrate or plate) | USPAT | 2004/04/13 13:00 |
| 27 | 1 | ("6440801").PN. | USPAT | 2004/04/13 12:56 |
| 28 | 1 | (("6440801").PN.) and (memory or cell or portion or first or second or all or height or 0.15 or microns or plurality or expose or exposed or side or buried or oxide or insulator or capacitor or FET or rails or pair or electorde or gate or DRAM or dual or gate or soft or error or enhanced or dielectric or substrate or plate) | USPAT | 2004/04/13 13:00 |
| 29 | 1 | ("5929477").PN. | USPAT | 2004/04/13 13:00 |
| 30 | 1 | (("5929477").PN.) and (memory or cell or portion or first or second or all or height or 0.15 or microns or plurality or expose or exposed or side or buried or oxide or insulator or capacitor or FET or rails or pair or electorde or gate or DRAM or dual or gate or soft or error or enhanced or dielectric or substrate or plate) | USPAT | 2004/04/13 13:01 |
| 31 | 1619 | 438/239 | USPAT | 2004/04/13 13:02 |
| 32 | 1506 | 438/240 | USPAT | 2004/04/13 13:02 |
| 33 | 1104 | 438/241 | USPAT | 2004/04/13 13:02 |
| 34 | 321 | 438/242 | USPAT | 2004/04/13 13:02 |
| 35 | 920 | 438/243 | USPAT | 2004/04/13 13:02 |
| 36 | 597 | 438/244 | USPAT | 2004/04/13 13:02 |
| 37 | 277 | 438/246 | USPAT | 2004/04/13 13:02 |

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|---|---|---|---|---|
| 38 | 298 | 438/248 | USPAT | 2004/04/13 13:02 |
| 39 | 570 | 438/250 | USPAT | 2004/04/13 13:03 |
| 40 | 3217 | 438/253 | USPAT | 2004/04/13 13:03 |
| 41 | 724 | 438/266 | USPAT | 2004/04/13 13:03 |
| 42 | 918 | 438/270 | USPAT | 2004/04/13 13:03 |
| 43 | 337 | 438/278 | USPAT | 2004/04/13 13:03 |
| 44 | 350 | 438/283 | USPAT | 2004/04/13 13:03 |
| 45 | 2363 | 438/305 | USPAT | 2004/04/13 13:03 |
| 46 | 876 | 438/306 | USPAT | 2004/04/13 13:03 |
| 47 | 324 | 438/311 | USPAT | 2004/04/13 13:04 |
| 48 | 1047 | 438/381 | USPAT | 2004/04/13 13:04 |
| 49 | 884 | 438/386 | USPAT | 2004/04/13 13:04 |
| 50 | 461 | 438/387 | USPAT | 2004/04/13 13:04 |
| 51 | 624 | 438/393 | USPAT | 2004/04/13 13:04 |
| 52 | 157 | 438/394 | USPAT | 2004/04/13 13:04 |
| 53 | 3147 | 438/396 | USPAT | 2004/04/13 13:04 |



4/13/04